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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/601,005	06/20/2003	Makoto Kudo	81751.0061	5768

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EXAMINER	
LAI, VINCENT	
ART UNIT	**PAPER NUMBER**
2181	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/02/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/601,005	KUDO, MAKOTO	
	Examiner	Art Unit	
	Vincent Lai	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 November 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 September 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Acknowledgement is made of the amendment to the claims and drawings filed by the applicant on 20 September 2006.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 20 September 2006 has been entered.

Drawings

3. The drawings were received on 20 September 2006. The Examiner accepts these drawings.

Priority

4. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). Certified copies of the priority documents have been received.

Information Disclosure Statement

5. The information disclosure statement (IDS) submitted on 4/22/2005 was considered by the examiner.

Response to Arguments

6. Applicant's arguments with respect to claims 1-18 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Dowling (U.S. Patent # 6,157,988).

As per **claim 1**, Dowling discloses a data processing device using pipeline control, comprising:

an instruction queue in which a plurality of instruction codes is fetched (See column 10, lines 37-45: Instructions fetched are stored together);

a fetch address operation circuit which calculates a fetch address used to fetch an instruction code in the instruction queue (See column 10, lines 10-13: Fetch addresses are calculated);

a fetch circuit which fetches an instruction code that is read out based on the fetch address into the instruction queue (See column 16, lines 3-14: Fetching is done by hardware using instructions); and

a branch information setting circuit which decodes a branch setting instruction, wherein the branch setting instruction explicitly or implicitly specifies a branch address (See column 10, lines 13-15: An offset is used to figure out the branch address) and a branch target address (See column 10, lines 55-58: Calculations are deemed implicit specifications as circuit must use instruction to perform calculations), when the fetch address is the branch address after x-th instruction from the branch setting instruction (See column 10, lines 13-15: An offset is used to figure out the branch address), the branch information setting circuit stores the branch address in a branch address storage register, and stores the branch target address in a branch target address storage register, when the branch setting instruction is decoded (See column 13, lines 29-34: Branching information is stored in registers);

wherein the fetch address operation circuit includes a circuit which compares one of a previous fetch address and an expected next fetch address with a value stored in the branch address storage register, and then determines whether or not to output a value stored in the branch target address storage register as a next fetch address,

based on the comparison result (See column 13, lines 2-14: Branch target address comparisons are made to determine whether to output information from saved data).

As per **claim 2**, Dowling discloses all but the last paragraph of the claim for reasons similar to that of claim 1. Dowling also discloses a data processing device using pipeline control comprising:

wherein the fetch address operation circuit includes a circuit which compares an expected next fetch address obtained by incrementing a value in a fetch program counter by one instruction length with a value stored in the branch address storage register, and then outputs a value stored in the branch target address storage register as a next fetch address when the expected next fetch address coincides with the value in the branch address storage register, or outputs the expected next fetch address as a next fetch address when the expected next fetch address does not coincide with the value in the branch address storage register (See column 16, lines 25-30: A non-delayed branch instruction is the offset branch address instruction).

As per **claim 3**, Dowling discloses the data processing device as defined in claim 1, wherein:

the branch setting instruction includes a loop instruction which designates a loop count (See column 18, lines 1-28: A counter is used with looping transitions);

the branch information setting circuit decodes the loop instruction which instructs to repeat a branch to the branch target address the number of times equal to the loop

count (See column 18, lines 1-28: A loop counter will repeat until it has reached zero), and stores the loop count designated by the loop instruction (See column 14, lines 13-19: A loop count has to be specified); and

the fetch address operation circuit includes a circuit which outputs a value stored in the branch target address storage register as a next fetch address until the number of times the branch to the branch target address repeats reaches the loop count (See column 18, lines 1-28: The loop counter is a determining factor for fetching).

Claim 4 is rejected for reasons similar to that of claim 3. Claim 4 has the same limitations as that of claim 3.

As per **claim 5**, Dowling discloses all but the last paragraph of the claim for reasons similar to that of claim 3. Dowling also discloses a data processing device using pipeline control comprising:

the fetch address operation circuit includes a circuit which decrements a value set in the loop counter each time when a branch to the branch target address occurs, and outputs a value obtained by incrementing the branch address by one instruction length as a next fetch address when the value of the loop counter reaches zero (See column 18, lines 1-28: The counter is not limited to just branch addresses and can also be used for branch target addresses).

Claims 6-8 are rejected for reasons similar to that of claim 5. Claims 6-8 have the same limitations as that of claim 5.

As per **claim 9**, Dowling discloses the data processing device as defined in claim 3, wherein:

the loop instruction has the branch target address which is fixed relative to the loop instruction and also has no branch target address information in an operand (See column 10, lines 15-17: Branch target address has to be calculated and thus would not be in the operand); and

the branch information setting circuit includes a circuit which calculates the value fixed relative to the loop instruction and stores the calculated value in the branch target address storage register (See column 10, lines 13-15 and column 13, lines 29-34: An offset is used to figure out the branch address, the branch address which is stored in registers).

Claims 10-12 are rejected for reasons similar to that of claim 9. Claims 10-12 have the same limitations as that of claim 9.

As per **claim 13**, Dowling discloses electronic equipment comprising:

the data processing device (See column 18, lines 39-43: Pipeline is meant to be used in a processor);

means for receiving input data (See column 9, lines 60-62: An input is necessary); and

means for outputting a result of processing the input data by the data processing device (See column 10, lines 64-65: After execution, data is put on data path to be stored).

Claims 14-18 are rejected for reasons similar to that of claim 13. Claims 14-18 have the same limitations as that of claim 13.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following patent is cited to show further art related to the application:

U.S. Patent # 6,311,261 B1 to Chamdani et al which teaches an apparatus and method for improving superscalar processors

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent Lai whose telephone number is (571) 272-6749. The examiner can normally be reached on M-F 8:00-5:30 (First BiWeek Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz M. Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vincent Lai
Examiner
Art Unit 2181

vl
January 25, 2007

DONALD SPARKS
SUPERVISORY PATENT EXAMINER